Amendments to the Claims

Please cancel Claims 5, 6 and 19 without prejudice to or disclaimer of the subject matter recited therein.

Please amend Claims 1, 7, 8, 10, 14, 17 and 18 to read as follows. Note that all the claims currently pending in this application, including those not presently being amended, have been reproduced below.

1. (Currently amended) An integrated-circuit apparatus comprising:

a CPU and a plurality of circuit blocks to be initialized in accordance with external reset signals and external clock signals, wherein

the circuit blocks each respectively output an initialization completion signal for communicating completion of initialization after the circuit blocks are initialized,

the CPU outputs an enable signal for permitting operations of the circuit blocks in accordance with the initialization completion signals output from the circuit blocks, ~~and~~

the circuit blocks are permitted to perform the operations by the enable signal, the external reset signals and the external clock signals, and

if there is any circuit block that is not initialized yet, the CPU initializes the circuit block by using the enable signal.

2. (Previously presented) The integrated-circuit apparatus according to claim 1, wherein

the circuit blocks are initialized to output the initialization completion signals, and said apparatus further comprises a logic circuit for inputting the initialization completion signals output from the circuit blocks to logic-operate the signals, and outputting the logic-operation results to the CPU.

3. (Original) The integrated-circuit apparatus according to claim 1, wherein

when all of the circuit blocks are initialized, the CPU outputs the enable signal to all the circuit blocks.

4. (Original) The integrated-circuit apparatus according to claim 2, wherein

when all of the circuit blocks are initialized, the CPU outputs the enable signal to all the circuit blocks.

Claims 5 and 6 (cancelled)

7. (Currently amended) The integrated-circuit apparatus according to ~~any one of claims 1 to 6~~ claim 1, wherein

the circuit blocks output the initialization completion signals when a predetermined period passes after the reset signal is input.

8. (Currently amended) The integrated-circuit apparatus according to any one of claims 1 to ~~6~~ 4, wherein

the integrated-circuit apparatus is constituted of one chip.

9. (Original) The integrated-circuit apparatus according to claim 7, wherein

the integrated-circuit apparatus is constituted of one chip.

10. (Currently amended) The integrated-circuit apparatus according to any one of claims 1 to ~~6~~ 4, wherein

the integrated-circuit apparatus is used for a printer.

11. (Original) The integrated-circuit apparatus according to claim 7, wherein

the integrated-circuit apparatus is used for a printer.

12. (Original) The integrated-circuit apparatus according to claim 8, wherein

the integrated-circuit apparatus is used for a printer.

13. (Original) The integrated-circuit apparatus according to claim 9, wherein

the integrated-circuit apparatus is used for a printer.

14. (Currently amended) An ink-jet recording apparatus comprising:

an integrated-circuit apparatus for controlling recording using a recording head, wherein

the integrated-circuit apparatus comprises a CPU and a plurality of circuit blocks to be initialized in accordance with external reset signals and external clock signals,

the circuit blocks each respectively output an initialization completion signal for communicating completion of initialization after the circuit blocks are initialized,

the CPU outputs an enable signal for permitting operations of the circuit blocks in accordance with the initialization completion signals output from the circuit blocks, ~~and~~

the circuit blocks are permitted to perform the operations by the enable signal, the external reset signals and the external clock signals, and

each of the circuit blocks is provided with a circuit to which the enable signal output from the CPU and the reset signals are input to be synchronized by the clock signals and the circuit outputs the enable signal to the circuit blocks.

15. (Previously presented) The ink-jet recording apparatus according to claim 14, wherein

the recording head comprises a control circuit and the circuit blocks each respectively output a signal for initializing the control circuit.

16. (Previously presented) The ink-jet recording apparatus according to claim 14, further comprising a driving circuit for performing the recording and the circuit blocks each respectively output a signal for initializing the driving circuit.

17. (Currently amended) A control method of an integrated-circuit apparatus having a CPU and a plurality of circuit blocks to be initialized in accordance with external reset signals and external clock signals, comprising the steps of:

initializing the circuit blocks;

outputting an initialization completion signal for communicating completion of initialization in the initializing step;

outputting an enable signal for permitting operations of the circuit blocks in accordance with the signal output in the initialization completion signal outputting step; ~~and~~

permitting the circuit blocks to perform the operations by the enable signal, the external reset signals and the external clock signals; and

if there is any circuit block that is not initialized yet, initializing the circuit block by using the enable signal.

18. (Currently amended) ~~The~~ An integrated-circuit apparatus ~~according to Claim 1,~~ comprising:

a CPU and a plurality of circuit blocks to be initialized in accordance with external reset signals and external clock signals, wherein

the circuit blocks each respectively output an initialization completion signal for communicating completion of initialization after the circuit blocks are initialized,

the CPU outputs an enable signal for permitting operations of the circuit blocks in accordance with the initialization completion signals output from the circuit blocks,

the circuit blocks are permitted to perform the operations by the enable signal, the external reset signals and the external clock signals, and

~~wherein~~ each of the circuit blocks is provided with a circuit to which the enable signal output from the CPU and the reset signals are input to be synchronized by the clock signals and the circuit outputs the enable signal to the circuit blocks.

Claim 19 (cancelled)